Claims

[c1] 1. An expansion output circuit for an embedded system comprising a host controller and a peripheral device, said expansion output circuit comprising:
a logic circuit coupled to first and second signals, generating an internal strobe signal in response to a transition between a first state and a second state of said first and second signals;
a register with clock signal coupled to said internal strobe signal and with input lines coupled to data signals from said host controller;
wherein said first and second signals are coupled to said peripheral and wherein all four states of said first and second signals are utilized by said peripheral;
wherein said host controller is configured to prevent a direct transition from said first state to said second state when changing the state of said first and second signals as necessary to perform input or output on said peripheral; and
wherein said host controller is configured to generate a direct transition from said first state to said second state to perform output to said register.

[c2] 2. The expansion output circuit according to Claim 1 wherein said logic circuit comprises the logical equivalent of a three-input AND gate coupled to said first and second signals and a delay element coupled to said second signal and to said three-input AND gate, wherein said internal strobe is coupled to the output of said three-input AND gate.

[c3] 3. The expansion output circuit according to Claim 1 wherein said logic circuit comprises the logical equivalent of a three-input AND gate coupled to said first and second signals, a delay element coupled to said second signal and to said three-input AND gate, a two-input AND gate coupled to said first signal, and a two-input OR gate coupled to said three-input AND gate and to said two-input AND gate, wherein the output of said two-input OR gate is coupled to said two-input AND gate and wherein said internal strobe is coupled to the output of said two-input OR gate.

[c4] 4. The expansion output circuit according to Claim 1 wherein:
said first state consists of the state when said first signal is at a logic low level and said second signal is at a logic low level; and
said second state consists of the state when said first signal is at a logic low level and said second signal is at a

logic high level.

[c5] 5. The expansion output circuit according to Claim 4 wherein to prevent said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) setting said first signal to a logic high state;
(b) setting said second signal to said second new state; and
(c) setting said first signal to said first new state.

[c6] 6. The expansion output circuit according to Claim 4 wherein to prevent said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;
(b) if said second previous state is not the same as said second new state, setting said second signal to said second new state; and
(c) if said first new state is not a logic high, setting said

first signal to said first new state.

[c7] 7. The expansion output circuit according to Claim 4 wherein to generate said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) setting said first signal to a logic high state;
(b) setting said second signal to a logic low state;
(c) setting said first signal to a logic low state;
(d) setting said second signal to a logic high state;
(e) setting said first signal to a logic high state;
(f) setting said second signal to said second new state; and
(g) setting said first signal to said first new state.

[c8] 8. The expansion output circuit according to Claim 7 further comprising the step of setting said data signals to a state consisting of desired output data before said step (d).

[c9] 9. The expansion output circuit according to Claim 4 wherein to generate said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to

a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;

(b) if said second previous state is not a logic low state, setting said second signal to a logic low state;

(c) setting said first signal to a logic low state;

(d) setting said second signal to a logic high state;

(e) setting said first signal to a logic high state;

(f) if said second new state is not a logic high state, setting said second signal to said second new state; and

(g) if said first new state is not a logic high state, setting said first signal to said first new state.

[c10] 10. The expansion output circuit according to Claim 9 further comprising the step of setting said data signals to a state consisting of desired output data before said step (d).

[c11] 11. The expansion output circuit according to Claim 4 wherein to generate said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal and said second signal to a logic low state;
(b) setting said second signal to a logic high state;
(c) setting said first signal to a logic high state; and
(d) setting said first signal and said second signal to said first new state and said second new state respectively.

[c12] 12. The expansion output circuit according to Claim 11 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

[c13] 13. The expansion output circuit according to Claim 4 wherein to generate said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) if said first previous state is not a logic low state, setting said first signal to a logic low state, and if said second previous state is not a logic low state, setting said second signal to a logic low state;
(b) setting said second signal to a logic high state;
(c) setting said first signal to a logic high state; and
(d) if said first new state is not a logic high state, setting said first signal to said first new state, and if said second

new state is not a logic high state, setting said second signal to said second new state.

[c14] 14. The expansion output circuit according to Claim 13 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

[c15] 15. The expansion output circuit according to Claim 4 wherein to generate said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) setting said first signal and said second signals to a logic low state;
(b) setting said second signal to a logic high state; and
(c) setting said first signal and said second signal to said first new state and said second new state respectively.

[c16] 16. The expansion output circuit according to Claim 15 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

[c17] 17. The expansion output circuit according to Claim 4

wherein to generate said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic low state, setting said first signal to a logic low state, and if said second previous state is not a logic low state, setting said second signal to a logic low state;

(b) setting said second signal to a logic high state; and

(c) if said first new state is not a logic low state, setting said first signal to said first new state, and if said second new state is not a logic high state, setting said second signal to said second new state.

[c18] 18. The expansion output circuit according to Claim 17 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

[c19] 19. An expansion input circuit for an embedded system comprising a host controller and a peripheral device, said expansion output circuit comprising:

a logic circuit coupled to first and second signals, activating an internal enable signal in response to a transition between a first state and a second state of said first

and second signals, and deactivating said internal enable signal in response to a transition between said second state and a third state of said first and second signals;
a buffer with enable signals coupled to said internal enable signal and with data output lines coupled to data signals from said host controller;
wherein said first and second signals are coupled to said peripheral and wherein all four states of said first and second signals are utilized by said peripheral;
wherein said host controller is configured to prevent a direct transition from said first state to said second state when changing the state of said first and second signals as necessary to perform input or output on said peripheral; and
wherein said host controller is configured to generate a direct transition from said first state to said second state, and to generate a direct transition from said second state to said third state to perform input from said buffer.

[c20] 20. The expansion input circuit according to Claim 19 wherein said logic circuit comprises the logical equivalent of a three-input AND gate coupled to said first and second signals, a delay element coupled to said second signal and to said three-input AND gate, a two-input AND gate coupled to said first signal, and a two-input

OR gate coupled to said three-input AND gate and to said two-input AND gate, wherein the output of said two-input OR gate is coupled to said two-input AND gate and wherein said internal enable is coupled to the output of said two-input OR gate.

[c21] 21. The expansion input circuit according to Claim 19 wherein:
said first state consists of the state when said first signal is at a logic low level and said second signal is at a logic low level;
said second state consists of the state when said first signal is at a logic low level and said second signal is at a logic high level; and
said third state consists of the state when said first signal is at a logic high level and said second signal is at a logic high level.

[c22] 22. The expansion input circuit according to Claim 21 wherein to prevent said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) setting said first signal to a logic high state;
(b) setting said second signal to said second new state;

and

(c) setting said first signal to said first new state.

[c23] 23. The expansion input circuit according to Claim 21 wherein to prevent said direct transition from said first state to said second state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;

(b) if said second previous state is not the same as said second new state, setting said second signal to said second new state; and

(c) if said first new state is not a logic high, setting said first signal to said first new state.

[c24] 24. The expansion input circuit according to Claim 21 wherein to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal to a logic high state;

(b) setting said second signal to a logic low state;
(c) setting said first signal to a logic low state;
(d) setting said second signal to a logic high state;
(e) setting said first signal to a logic high state;
(f) setting said second signal to said second new state; and
(g) setting said first signal to said first new state.

[c25] 25. The expansion input circuit according to Claim 24 further comprising the step of reading the state of said data signals between step (d) and step (e).

[c26] 26. The expansion input circuit according to Claim 21 wherein to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;
(b) if said second previous state is not a logic low state, setting said second signal to a logic low state;
(c) setting said first signal to a logic low state;
(d) setting said second signal to a logic high state;
(e) setting said first signal to a logic high state;

(f) if said second new state is not a logic high state, setting said second signal to said second new state; and
(g) if said first new state is not a logic high state, setting said first signal to said first new state.

[c27] 27. The expansion input circuit according to Claim 26 further comprising the step of reading the state of said data signals between step (d) and step (e).

[c28] 28. The expansion input circuit according to Claim 21 wherein to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) setting said first signal and said second signal to a logic low state;
(b) setting said second signal to a logic high state;
(c) setting said first signal to a logic high state; and
(d) setting said first signal and said second signal to said first new state and said second new state respectively.

[c29] 29. The expansion input circuit according to Claim 28 further comprising the step of reading the state of said data signals between step (b) and step (c).

[c30] 30. The expansion output circuit according to Claim 21 wherein to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state, said host controller changes the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:
(a) if said first previous state is not a logic low state, setting said first signal to a logic low state, and if said second previous state is not a logic low state, setting said second signal to a logic low state;
(b) setting said second signal to a logic high state;
(c) setting said first signal to a logic high state; and
(d) if said first new state is not a logic high state, setting said first signal to said first new state, and if said second new state is not a logic high state, setting said second signal to said second new state.

[c31] 31. The expansion input circuit according to Claim 30 further comprising the step of reading the state of said data signals between step (b) and step (c).